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**a.v**

module invert(input wire i, output wire o1);

assign o1 = !i;

endmodule

module and2(input wire i0, i1, output wire o2);

assign o2 = i0&i1;

endmodule

module or2(input wire i0, i1, output wire o3);

assign o3 = i0||i1;

endmodule

module xor2(input wire i0, i1, output wire o4);

assign o4 = i0^i1;

endmodule

module nand2(input wire i0, i1, output wire o5);

wire t;

assign o5 = !(i0&i1);

endmodule

**testbench.v**

module tb;

reg t\_a;

reg t\_b;

wire P,Q,R,S,T;

//instantiate

invert a1(.i(t\_a),.o1(P));

and2 a2(.i0(t\_a),.i1(t\_b),.o2(Q));

or2 a3(.i0(t\_a),.i1(t\_b),.o3(R));

xor2 a4(.i0(t\_a),.i1(t\_b),.o4(S));

nand2 a5(.i0(t\_a),.i1(t\_b),.o5(T));

initial begin $dumpfile("dmp1.vcd");

$dumpvars(0,tb);

end

initial begin $monitor(t\_a,t\_b,P,Q,R,S,T); //displays the content of the register

t\_a=1'b0;//1 bit input

t\_b=1'b0;

#10 //time nanosecs

t\_a=1'b0;//1 bit input

t\_b=1'b1;

#10 //time nanosecs

t\_a=1'b1;//1 bit input

t\_b=1'b0;

#10 //time nanosecs

t\_a=1'b1;//1 bit input

t\_b=1'b1;

#10 //time nanosecs

t\_a=0;//inorder to see the last input

t\_b=0;

end

endmodule

